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Threshold Voltage Shifts in Organic Thin-Film Transistors due to Self-Assembled Monolayers at the Dielectric Surface**

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Abstract

Recently, it has been shown by several groups that the electrical characteristics of organic thin-film transistors (OTFTs) can be significantly influenced by depositing self-assembled monolayers (SAMs) at the organic semiconductor/dielectric interface. In this work, the effect of such SAMs on the transfer characteristics and especially on the threshold voltage of OTFTs is investigated by means of two-dimensional drift-diffusion simulations. The impact of the SAM is modeled either by a permanent space charge layer that can result from chemical reactions with the active material, or by a dipole layer representing an array of ordered dipolar molecules. We demonstrate that in both model cases, the presence of the SAM significantly changes the transfer characteristics. In particular, it gives rise to a modified, effective gate voltage V_{eff} that results in a rigid shift of the threshold voltage, ΔV_{th}, relative to a SAM-free OTFT. The achievable amount of threshold voltage shift, however, strongly depends on the actual role of the SAM. While for the investigated device dimensions, an organic SAM acting as a dipole layer can realistically shift the threshold voltage only by a few volts, the changes in the threshold voltage can be more than an order of magnitude larger when the SAM leads to charges at the interface. Based on the analysis of the different cases, we propose a route to experimentally discriminate between SAM-induced space charges and interface dipoles. The developed model allows us to qualitatively describe the behaviour of organic transistors containing reactive interfacial layers; when incorporating rechargeable carrier trap states and a carrier density-dependent mobility, even a quantitative agreement between theory and recent experiments can be achieved.

1. Introduction

Over the past years, the interface between the organic semiconductor (OSC) and the dielectric in organic thin-film transistors has been the subject of numerous investigations. As organic transistors usually operate in accumulation mode and charge transport typically takes place in the first few mono-layers of the OSC adjacent to the gate dielectric,[1,2] the transistor performance is greatly influenced by properties of this interface. It has, for example, been shown that the carrier mobility in polycrystalline materials such as pentacene strongly depends on the morphology and the molecular ordering in the channel, which in turn is governed by the quality and the reactivity of the dielectric (i.e., oxide) surface.[3,4,5,6] Moreover, chemical reactions taking place at the OSC/dielectric interface were reported to create/annihilate carrier trap states that can shift the threshold-voltage by several ten volts.[7] Interface trap states at the SiO_x surface have also been identified as inhibiting n-type conduction in common device architectures.[8] Yoon et al. have presented a comprehensive experimental study on the correlation between the oxide surface chemistry and the threshold-voltage, mobility, current on-off ratio and sub-threshold slope for various p-type, n-type and ambipolar OTFTs.[9]

Recently, several groups reported that the electrical properties of organic transistors can be controlled via self-assembled mono-layers (SAMs) bearing different functional groups that align on the oxide surface. In this context, active layers deposited by physical vapor deposition[10,11] as well as solution processed active materials[12,13] have been investigated. Depending on the nature of the deposited SAMs, shifts of the threshold voltage by several ten volts and significant changes in the sub-threshold slope have been observed.

The experimental observations have commonly been attributed to SAMs acting as a dipolar layers, inducing a potential jump[11] caused by the electric field “within” the layer.[10,13] The presence of

such built-in fields has been confirmed by contact potential measurements.[14,15] Jang et al. have,[6] however, recently reported that merely changing the dipole moments of the molecules forming the SAM results in threshold voltage shifts of only a few volts. An alternative explanation can be based on the work by Scheinert et al.[16,17,18] They have shown by drift-diffusion based modeling that also interface traps or charged interfacial layers can result in threshold voltage shifts and changes in the sub-threshold slope. The latter has been confirmed by Bolognesi and DiCarlo [19].

The purpose of this paper is (i) to provide a detailed comparison between the impact of a dipolar and a space charge layer on the device characteristics, (ii) to develop an intuitive picture on how OTFTs containing interfacial layers operate, and (iii), based on that understanding, propose an experimental strategy that allows one to distinguish by which mechanism a particular SAM shifts the transfer characteristics of a device.

To that aim, we describe potential and carrier distributions as well as the resulting currents in various types of OTFTs by means of drift-diffusion based models. As a first step, an ideal device (i.e., a device without any interface modification) is described right after turn on and during steady state operation. This is crucial for being able to subsequently develop the picture describing devices containing either dipolar or charged interfacial layers. Finally, the calculations are compared to recent experiments by Pacher et al.,[12] who, for devices containing reactive interfacial layers,have described threshold voltage shifts from around +45 V to -12 V after exposing those devices to ammonia.

2. The device model

Typical geometries of OTFTs feature large aspect ratios, as illustrated schematically in **Figure 1**. Layer thicknesses are of the order of some 10 nm for the organic material and of around 100 nm for

the gate dielectric, respectively. While short channel devices with sub-µm channel lengths have been realized,[20] in most devices the channel length (i.e., the distance between source and drain electrodes) measures some 10 µm. The width of the device, on the other hand, often is in the mm regime. It is the huge width/length ratio that allows for the simulation of charge transport on a two-dimensional cross-section of the device. Therefore, simulations have been performed for the 2D device cross-section shown in the right part of Figure 1, which also summarizes the actually chosen device dimensions (width W=7 mm, channel length L=10 µm, source (drain) overlap with gate y_s=2 µm, OSC thickness d_{osc}=30 nm, oxide thickness d_{ox}=100 nm).

These simulations have been carried out for top-contact transistor structures. It is, however, important to note at this point that simulations of bottom-contact designs yielded the same threshold voltage shifts induced by permanent space charges and interface dipoles. The focus is on devices that feature holes as the majority charge carriers, i.e., electron transport is assumed to be negligible. Our approach is based on modeling the temporal evolution of the electric potential and the carrier density in typical OTFT geometries by a system of three equations, consisting of the continuity equation, the drift-diffusion equation and the Poisson equation.[21] Temporal changes of a given initial hole density $p_0(x,y)=p(x,y,t=0)$ in the OTFT are computed via the continuity equation,

$$\frac{\mathrm{d}p(x,y,t)}{\mathrm{d}t} + \frac{1}{e}\nabla \cdot \mathbf{j}(p,\mathbf{E}) = 0 \qquad (1)$$

Here, $p(x,y,t)$ is the hole density, e stands for the elementary charge and $\mathbf{j}(p,\mathbf{E})=[j_x(p,E_x), j_y(p,E_y)]$ denotes the two-dimensional vector of the current density. The motion of charges $\mathbf{j}$ is controlled via the drift-diffusion equation,

$$\mathbf{j} = ep\mu\mathbf{E}(x,y,p) - \frac{k_B T \mu}{e}\nabla p \qquad (2)$$

where μ symbolizes the carrier mobility, $\mathbf{E}(x,y,p)$ indicates the electric field, k_B is the Boltzmann constant and T denotes the temperature. The first term in (2) describes the drift of holes due to an

electric field and the second term accounts for diffusion caused by local differences in the carrier concentration. Throughout the conceptual discussion of interface effects in Sections 3.1 and 3.2, the mobility is held constant, i.e., μ=4.0×10^{-4} cm^{2}V^{-1}s^{-1}.[22] Later, when comparing the results to actual experimental data, the mobility is treated as carrier-density-dependent in order to reproduce measurements in fine detail (further details will be given in Section 3.3). The electric field is determined by the negative gradient of the electric potential, $\mathbf{E}=-\nabla\varphi$, which is governed by the Poisson equation,

$$\nabla \cdot \left[\varepsilon_r(x)\nabla\varphi\right] = \frac{e}{\varepsilon_0}\left[N_A - p - \frac{N_{fix}(x,y)}{e}\right] \qquad (3)$$

Here, $\varepsilon_r(x)$ is the relative permittivity of the respective layer, ε_0 the electric constant, N_A the acceptor doping density and $N_{fix}(x,y)$ denotes the term in which permanent space charge layers and dipole densities can be incorporated.

For obtaining the numerical solution of the system (1)-(3), the physical state of an OTFT is mathematically characterized by initial and boundary conditions for the occurring quantities. Further details on the developed code for the self-consistent solution of the given initial value problem (1)-(3) are presented in section 5 (Computational details).

In equation (3), permanent space charge layers at the OSC/dielectric interface ($x=x'$ in the right part of Figure 1) can be readily incorporated. The term $N_{fix}(x,y)$ then reads

$$N_{fix}(x,y) = \sigma_{if}\delta(x-x') \qquad (4)$$

where σ_{if} is the surface-density of the fixed surface charge and δ is the Dirac delta function. An interface dipole is modeled similarly to equation (4), but with two equal surface charge densities σ_{dip} of opposite signs at the distance $d_{dip}=x''-x'$, leading to

$$N_{fix} = -\sigma_{dip}\delta(x-x') + \sigma_{dip}\delta(x-x'') \qquad (5)$$

The concept of two parallel surface charge densities, as stated in equation (5), should be suitable for modeling the electrostatic impact of a polarized SAM at the OSC/dielectric interface independent of the microscopic origin of the molecular dipole. The dipole density $\gamma=\sigma_{dip}d_{dip}$ is then related to the dipole moment M_{dip} of a single molecule in the SAM via

$$\gamma = d_{dip}\sigma_{dip} = \frac{M_{dip}}{A} \qquad (6)$$

where A denotes the area of a single molecule on the surface.

3. Results and discussion

3.1. Operation regimes of OTFTs

Prior to studying the impact of SAMs at the OSC/insulator interface, it is useful to investigate in detail how the transfer characteristics, i.e., the dependence of the drain current I_D on the gate voltage V_G, and the threshold voltage, V_{th}, are related to the charge carrier density and electric potential distributions in a pristine device under operation. The term V_{th} here is used in the spirit of Meijer et al.,[23] representing the gate voltage at which the transport band at the OSC/dielectric interface is completely flat.

A qualitative understanding of the different operation regimes of an OTFT can be already obtained from representative electric potential profiles. We will first discuss the situation immediately after switching the transistor from flat-band condition to a particular state, i.e., at simulation time t = 0 ps, prior to the injection of any mobile carriers. At that stage, a steady state has not yet been established. The potential distributions are shown in **Figure 2** for V_{DS}=-20 V and for the gate voltage chosen to represent a) the off state (V_G = 14 V), b) the flat-band condition, where in the present case V_G equals V_{th} (V_G=0 V), c) the saturation regime, where $|V_G|<|V_{DS}|$ (V_G = -12 V), and d) the linear regime, where $|V_{GS}|>|V_{DS}|$ (V_G = -50 V).

In accordance with an earlier study by Tessler and Roichman,[24] in all four cases, there is no electric field in nearly the entire channel region. The portion of the channel in which the potential is flat will be referred to as the zero-field region. There, the potential matches the one applied at the gate contact. This situation is a consequence of the large aspect ratio of the considered OTFT cross-section, here L/d equals $10/0.13 \approx 77$ (note the different scales of the x- and y-axes in Figure 2). When the transistor is turned off ($V_G > V_S > V_D$; Figure 2a) the zero-field region lies above the source and drain potentials. In that case, no holes can overcome the resulting barriers and, thus, cannot enter the channel. When decreasing the gate voltage to 0 V, i.e., in the flat-band situation shown in Figure 2b, the entrance barrier at the source edge vanishes exactly; in this case, V_G is identical to the threshold voltage V_{th}. Decreasing the gate voltage further results in the device being operated in the saturation regime (Figure 2c); as the zero-field region now lies energetically between the source and drain electrodes, holes can enter the channel from the region under the source, where carriers will accumulate at the OSC/dielectric interface within some picoseconds. The electric field below the drain contact forces each arriving carrier to be immediately ejected into the electrode. In the linear regime, shown in Figure 2d, holes are initially able to enter the channel from both the source and drain sides. Therefore, both electrodes act as injecting contacts for a short period of time, i.e., until a non-vanishing source-drain electric field has been established (see below).

When further progressing in time, a steady state is reached. The linear and saturation regimes differ significantly from the initial situations shown in Figure 2. The resulting electric potential distributions over the device cross-section are shown in the left part of **Figure 3.** The corresponding hole density distributions are depicted to their right on a logarithmic scale for the active region only (i.e., only for the region between x = 0 µm and 0.03 µm). Injected carriers accumulate at the OSC/dielectric interface, i.e., a channel is formed in both regimes. This charge accumulation leads to a slope of the potential between source and drain (Figure 3a, c) and thus to an electric field that

drives a current through the device. At a first glance, it might appear counter-intuitive that charge carrier accumulation is needed for the establishment of this driving field although a voltage is always applied between source and drain; at this point, however, it needs to be stressed again that this is a consequence of the extreme aspect ratio of an OTFT. In the absence of free charges at the interface to the dielectric that can "screen" the gate potential, the potential in the channel region is solely determined by the gate voltage. The interface charge density adopts its maximum in the region of the channel directly under the source contact (*cf.* Figure 3b, d). It is given by

$$\sigma_{\max} = -V_G C_{ox} \qquad (7)$$

In the linear regime (Figure 3a), a continuous decrease of the channel potential and the carrier density (Figure 3b) from source to drain (note the logarithmic scale in the right part of Figure 3a) is observed. This situation changes drastically in the saturation regime. The channel in the vicinity of the drain electrode is depleted of charge carriers (the so-called pinch-off) (right part of Figure 3b). Considering that the steady state current is constant across the entire device, a drop in carrier density (and, thus, conductivity) gives rise to large local electric fields and, consequently, to a large potential drop close to the drain edge (y=12 μm in Figure 3b). As a consequence of the large aspect ratio of the device, this pinch-off is always confined to a comparatively narrow region close to the drain edge. Note that a similar potential drop at the *source edge*, which is frequently observed in experiments,[25,26] can be reproduced in our calculations by implementing an injection barrier at the source/drain electrodes (details in section 5).

3.2 OTFT containing electronically "active" interfacial layers

Having reviewed the fundamental description of OTFT operation, we now turn to the investigation of devices in which the properties of the interface between the gate dielectric and the active layer have been modified. First, we discuss the consequences of including an additional permanent space charge layer at the OSC/dielectric interface, originating, e.g., from a chemical reaction of the SAM

with the active layer[12] or from permanently filled trap states. In **Figure 4** the electric potentials at t=0 ps and in steady state are depicted at V_{DS}=-20 V for a fixed surface charge of σ_{if}=-6×10^{12} ecm^{-2} according to equation (4) and for V_G=0 V. The chosen value of σ_{if} corresponds to a 1.5%-ionization of the SAM, assuming a footprint of each molecule of 25 Å^2. Figure 4a displays the charge neutral initial state, i.e., in the instant when the gate bias has just been applied. The region with vanishing electric field (2 < y < 12 μm; 0 < x < 0.03μm) lies at a potential that is significantly different from the one applied to the gate; this strongly contrasts the situation in the pristine device in Figure 2b, although the same voltages are applied to the electrodes. Comparing the potential distributions in Figure 2d and Figure 4a, it becomes obvious that the transistor now operates in the linear regime despite the gate voltage being zero. This can be modeled by an *effective* gate potential, V_{eff}. In accordance with our simulations, it is given by

$$V_{eff} = V_G + \frac{\sigma_{if}}{C_{ox}} \qquad (8)$$

and corresponds to V_G being shifted by an additional voltage drop σ_{if}/C_{ox}. The latter is simply a consequence of the continuity requirement for the displacement field across the interface (Gauss' law). In a more intuitive approach, it can be interpreted as the voltage drop across a capacitor that is formed by (i) the space charge layer at interface to the OSC and (ii) the opposite charge density induced in the gate contact at the other side of the *dielectric layer*. Consequently, while the dielectric is field free in Figure 2b), there is a homogeneous field in the gate dielectric in Figure 4a. In this context, it should be mentioned that the reason why the present transistor operates in the linear regime at V_G = 0 and V_D = -20 V is that $|V_D| < |V_{eff}|$. At reduced negative interface charge densities, saturation type operation at V_G = 0 V would be observed. In the case of a positive interface charge, the transistor would be turned off at V_G = 0 V, since then $V_{eff} > V_S$=0 V.

A similar situation is also encountered in the steady state operation of the device (Figure 4b). Again, the potential distribution (and consequently also the distribution of free carriers) in the active layer is equivalent to the case depicted in Figure 3a), in spite of the different gate voltages and fields within the dielectric. In analogy to equation (7), the maximum value of the accumulated interface charge is determined by the effective gate voltage and the capacitance of the dielectric via:

$$\sigma_{\max} = -V_{eff} C_{ox} \qquad (9)$$

Consequently, a fixed space charge layer at the OSC/dielectric interface results in a rigid shift of the transfer characteristics by $\Delta V_{\text{th}} = \sigma_{if}/C_{ox}$ with respect to an ideal reference device. This can also be seen in the comparison between simulated transfer curves in **Figure 5** with (circles) and without (diamonds) incorporating σ_{if}. The threshold voltages that can be extracted from these curves following the model of Horowitz et al.[27] agree excellently with the values predicted according to equation (8). Threshold voltages obtained from the simulated transfer characteristics are compared with effective gate voltages at V_G=0 V, obtained from equation (8), in **Table 1** for different interface charge densities. For example, a space charge layer with σ_{if}=-6×10^{12} ecm^{-2} causes a shift of 28 V. As such charge densities are certainly realistic for SAMs consisting of molecules that strongly interact with the active material and are also conceivable for interface trap densities, this result implies that interfacial space charge layers can, indeed, shift the transfer characteristics of OTFTs with common device dimensions by several ten volts.

As a next step, the role of a dipole layer at the OSC/dielectric interface is investigated. It is modeled by two parallel surface charge densities $\pm\sigma_{dip}$ at a distance of d_{dip}=0.8 nm, right between the active region and the gate dielectric according to equation (5). This situation is depicted in Figure 1. A priori, one would expect a potential drop, $\Delta\varphi_{dip}$, across such a dipole layer according to the Helmholtz equation[28]

$$\Delta\varphi_{dip} = \frac{d_{dip}\sigma_{dip}}{\varepsilon_0\varepsilon_{dip}} = \frac{M_{dip}}{\varepsilon_0\varepsilon_{dip}A} \quad (10)$$

where $\varepsilon_{\mathrm{dip}}$ denotes the effective dielectric constant present in the dipole layer (*vide supra*). In **Figure 6**, the electric potentials for V_G = 0 V at t=0 ps and in steady state are shown that were obtained with two surface charge densities σ_{dip} equal to $\pm 10^{14}$ ecm^{-2}, separated by 0.8 nm. These values correspond to an interface dipole density γ=3.84×10^{15} Dcm^{-2} and to a dipole moment of M_{dip}=9.6 Debye per molecule of a polar SAM, assuming a footprint of 25 Å^2 per molecule (see eq. 6). When comparing Figure 6a with the situation found in the pristine device (Figure 2) for the same biases, it is seen that the OTFT now operates in the saturation regime (*cf*. Figure 2c). The dipole layer has the same effect as if the *gate potential* was altered by $\Delta\varphi_{dip}$. In analogy to the case of the space charge layer, one can define an effective gate potential

$$V_{eff} = V_G \pm \Delta\varphi_{dip} \quad (11)$$

The direction of the shift is related to the orientation of the dipoles, i.e., the shift is negative if the negative side of the dipole is closer to the source (drain) electrode than the positive.

The potential jump $\Delta\varphi_{dip}$ from equation (10) must be accomodated within each potential cross-section perpendicular to the transistor surface. Nevertheless, such potential profiles, shown in Figure 6b, markedly differ underneath the contact (y=1 μm) and in the zero-field region (y=8.2 μm). At the instant the gate voltage is applied (t=0), the potential in the zero-field region (crosses in Figure 6b) exactly adopts the value -$\Delta\varphi_{dip}$. When establishing the steady state (triangles in Figure 6b), charges are accumulated in the cannel and thus the channel potential increases. Consequently, a source-drain electric field (y-direction) is established (Figure 6c). Under the source/drain contacts, however, the potential profile is restraint by the externally applied biases V_{GS}/V_{GD} at all times (squares and circles in Figure 6b). In the absence of mobile carriers at t=0, an electric field is established between the source contact (x=0) and the OSC/dielectric interface (x=0.03 μm). To

reach the steady state, charges accumulate at the interface until this electric field vanishes. The upper bound of the accumulated charge σ_{max} under the contact is, thus, given by equation (9) with V_{eff} from equation (11).

Consequently, a dipole layer at the OSC/dielectric interface results also in a rigid shift of the transfer characteristic with respect to an ideal reference device. This can be seen from the comparison between simulated transfer curves in Figure 5 without (diamonds) and with (stars) an interfacial dipole density γ=3.84×10^{15} Dcm^{-2}. The excellent correspondence between the threshold voltage shifts extracted from the simulated transfer characteristics with the ones expected from equation (11) is summarized in **Table 2** [29] for interfacial dipole densities γ varying between 2×10^{15} and 2×10^{16} Debye per square centimeter.

Having related both the charged and dipolar interfacial layers to the occurrence of an effective gate voltage V_{eff}, we can now compare their quantitative impact on V_{th}. From the above considerations (and the values in Table 2), the molecular dipole moments necessary to induce a specific shift in the threshold voltage can be estimated. Here, we assume an idealized case of perfectly aligned and densely packed layers characterized by a molecular footprint of 25 Å^2. [30,31] The resulting M_{dip} as calculated from equation (6) are also contained in Table 2. Dipole moments of polar molecules used to modify the energetics of insulators or metal electrodes typically amount to only a few Debye.[12,19,32] According to Table 2, they can thus cause threshold voltage shifts on the order of 1.0-2.5 V in agreement with the experiments of Jang et al.[6] To explain shifts in V_{th} of up to 60 V, as observed, e.g., in Ref. [12] for organosilane modified OTFTs, in terms of a dipole layer, one, however, needs to assume molecular dipole moments that exceed 50 Debyes.[33] Considering that such unrealistically large M_{dip} values would be necessary,[34] we rule out that a dipole layer associated with the formation of an organic SAM can be the origin of threshold voltage shifts of

some ten volts. Rather, SAM-related space charge layers, for which such shifts can be expected under realistic conditions (*vide supra*), must be held responsible.

Based on the above considerations, an experimental approach that allows to unambiguously distinguish whether an observed threshold voltage shift exists due to a dipole layer or a space charge layer can be proposed. According to Horowitz et al.,[27] the source-drain current in OTFTs is directly proportional to the capacitance of the gate dielectric. This fact is reflected by equation (9), which states a linear dependence of the carrier density (and thus the conductivity) in the channel on the oxide capacitance. Thus, in a device with a "clean" interface, i.e., $V_{th} \approx 0$ V, increasing/decreasing the oxide capacitance causes a proportional increase/decrease of the current in the transfer characteristics. Altering the capacitance can be achieved, for example, by using substrates with varying oxide thickness or by changing the relative permittivity of the dielectric. In a device containing an electrically active interfacial layer, i.e. $|V_{th}| >> 0$ V, altering C_{ox} can have an additional effect: if a space charge layer σ_{if} is the origin of the non-zero threshold voltage, according to equation (8), the threshold voltage is inversely proportional to the oxide capacitance. In contrast, if a dipolar layer is present at the OSC/dielectric interface, according to (12), the threshold voltage is not affected by a change of the oxide capacitance. This can intuitively be understood from the fact that in the case of a space-charge layer it is the voltage drop over the dielectric that determines the threshold voltage shift, while in the case of a dipolar layer, it is the voltage drop over exactly that layer that matters.

3.3 Comparison with experimental data

Having reached a semi-quantitative understanding of how a SAM influences the threshold voltage, we now turn to the simulation of a real device to check the extent to which the measured transfer characteristics can be quantitatively reproduced. Below, we consider top-contact transistors with

setup and dimensions as in the ones fabricated by Pacher et al. [12] as experimental reference. These OTFTs are made of 10 nm regioregular poly(3-hexylthiophene) (rr-P3HT) as the active material deposited onto approximately 2 nm thick SAMs covalently linked to 170 nm of SiO_2 as the gate dielectric. Au top contact source and drain electrodes are used. Logarithmic and linear plots of the measured transfer characteristics for V_{DS}= -45 V are depicted in **Figure 7** for two types of SAMs. The OTFT containing a n-hexadecyltrichlorosilane (HDTS) SAM is characterized by a steep sub-threshold slope and a threshold voltage close to zero; a SAM comprised of 4-(2-(trichlorosilyl)ethyl)benzene sulfonic acid chloride and its sulfonic acid analogue (T-SC/SA) leads to a threshold voltage of +45 V and a considerably shallower sub-threshold slope. The HDTS layer is known to shield the active material from traps at the SiO_2 surface,[8] providing an almost charge neutral interface between the OSC and the SAM-covered dielectric. However, the T-SC/SA layer must have changed the interface properties so that the transistor still operates in the saturation regime even at zero gate voltage.

Considering that the dipole moments related to the T-SC/SA molecules range between 2-4 D,[12] we omit their influence and model both OTFTs only with interfacial space charge layers determined from equation (8). The values of further input parameters required for the simulation, such as the mobility, are chosen to represent the above mentioned materials and are given in the Computational Details section.[12] The results of the simulations are compared to the experimental data in Figure 7. Above threshold, excellent agreement is obtained for the case of the HDTS layer with a small positive σ_{if} of $+1.0\times10^{12}$ ecm^{-2}, indicating that this transistor operates similar to the model OTFT from section 3.1 (discussing possible origins of a non-vanishing off-current is not a topic of the present paper).

For the T-SC/SA layer, the most accurate simulation with σ_{if}=-5.0×10^{12} ecm^{-2} does reproduce the main observation of a high positive threshold voltage. However, it fails to provide a full quantitative description of the experimental data. One deviation is the smaller sub-threshold slope in the experimental data. It is known to originate from rechargeable trap states.[17] Bearing in mind that the T-SC/SA layer reacts chemically with the active material,[12] the occurrence of an increased number of trap states in the T-SC/SA containing device, indeed, appears reasonable. Thus, as a next step, we also included a density of rechargeable interface traps N_t at energy ΔE from the valence band (details in section 5). Moreover, the experimental data indicate a non-linear dependence of the drain current on the gate voltage in the linear regime (i.e., at large negative gate voltages). This has been attributed to a carrier density-dependent mobility $\mu=\mu[p(x,y,t)]$ that needs to be considered in equation (2).[35] The more negative the gate voltage becomes, the more carriers accumulate in the channel, which leads to an increased mobility and a superlinear increase of the current. As the maximum currents for the T-SC/SA containing device are about a factor of 5 larger than in the device containing a HDTS layer, such effects can be expected to play a more significant role there. Therefore, a carrier concentration dependent model for the hole mobility has also been implemented. We adopted the model elaborated by Pasveer et al.[36], in which a minimum mobility μ_0 is varied exponentially with the width, σ, of a Gaussian broadened density of states (details in section 5). Both parameters μ_0 and σ can be viewed as fit parameters, which are set to values that most accurately reproduce the experimental data. With the incorporation of these refinements in our simulation, a quantitatively satisfying agreement between experiment and simulations is achieved also for the device containing the T-SC/SA layer (as depicted in **Figure 8** both on a linear as well as on a logarithmic scale), when choosing the following parameters: σ_{if}=-5.0×10^{12} ecm^{-2}, μ_0=1.0×10^{-8} cm^{2}V^{-1}s^{-1}, σ=2.9 k_BT, N_t=5×10^{13} cm^{-2}, ΔE=0.3 eV. In this context, it needs to be stressed that σ_{if} corresponds to an actual interfacial charge density, while N_t describes a density of trap states. Typically, only a very small fraction of those states is occupied with the occupation probability

being gate voltage dependent (see methodology). In particular, at negative gate voltages, the filling of the (acceptor) traps and thus their influence on the current are negligible. With V_G approaching the threshold voltage, more and more traps get filled and above V_{th} the resulting additional negative interface charge leads to a non-vanishing off-current and a smoother subthreshold slope. Only in this regime, the number of occupied trap states exceeds σ_{if}.

Furthermore, as expected, the carrier density-dependent mobility leads to a non-linear slope of the transfer characteristic in the linear regime. An even better agreement could be reached by incorporating more trap levels of various densities at different energies and by incorporating leakage currents, both not considered here. At this point, it needs to be stressed that the extensions to the general model that have been implemented in this last section (and those having been omitted) constitute improvements for the description of the actual shape of the transfer characteristics. They are not directly relevant for the qualitative conclusions, in particular how space charges and dipole layers affect the threshold voltage.

4. Summary and conclusions

Two-dimensional simulations on organic thin film transistors have been carried out on the basis of the drift-diffusion equations. In particular, we focused on how the influence of a self-assembled monolayer (SAM) at the interface between the dielectric and OSC on the transfer characteristics can be understood. Following scenarios suggested in literature, we modeled the presence of a SAM by including a constant space charge layer that can be formed due to chemical reactions between the SAM and the active material[12] or by charged traps whose occupation does not change when sweeping the gate voltage. Alternatively,[10,11,13] we described it as a layer of permanent dipoles at the dielectric/OSC interface.

When solely considering the impact of both model scenarios on the transfer characteristics a similar scenario evolves: The presence of either a charged or dipolar interfacial layer leads to a shift of the threshold voltage, V_{th}, and thus also of the transfer characteristics, $I_D(V_G)$, without affecting its overall shape. Analyzing, however, the microscopic origin of that shift reveals fundamental differences. Charges at the interface between the dielectric and the OSC induce opposite charges in the gate electrode and the ensuing field in the dielectric results in a threshold voltage shift. In the "dipole case" it is the potential discontinuity at an extended dipole layer that results in the shift of the threshold voltage. Being aware of that, one can suggest a test experiment to differentiate between the two effects in actual devices: When increasing the capacitance of the gate dielectric (either by decreasing its thickness or increasing its dielectric constant) the drain current at a particular gate voltage in excess of the threshold voltage will increase in both cases, while only in the presence of an interfacial space charge layer this will also result in a shift of the threshold voltage. Our calculations also imply that the experimentally observed threshold voltage shifts of several ten volts can be explained by realistic interfacial charge densities, while the necessary molecular dipole moments would have to be more than an order of magnitude larger than those of common SAM-forming molecules.

The applied model allows a good qualitative description of observed threshold voltage shifts. Minor quantitative deviations of this simple model from experimental data for SAM-containing poly(thiophene) based transistors can be accounted for by including rechargeable trap states as well as a carrier-density dependence of the mobility in our calculations.

5. Computational details

In order to self-consistently solve the initial value problem given by the equations (1)-(3), a five-point finite difference scheme on a predefined grid with variable mesh-spacing was

implemented.[21] The spacing was adapted to the special OTFT geometry depicted in Figure 1, i.e., the mesh cell lengths perpendicular to the transistor surface typically are two orders of magnitude smaller than their parallel extensions. At critical positions, such as the OSC/dielectric interface or the source/drain contacts and their edges, a particularly fine mesh was implemented. Such refinements lead to large variations for the cell extensions perpendicular to the surface: Starting out from ca. 100 points per μm in the dielectric, the resolution was typically increased by a factor of 5 in the OSC and by an additional factor of ca. 20 at the OSC/dielectric interface and close to the contacts. The latter resolution with cell lengths of down to a few Å is required to guarantee the accurate description of the interface and dipole layer charges.

For the Poisson equation (3), the system of linear equations resulting from the finite difference approach was solved by an iterative Gauss-Seidel algorithm.[21] The potential at the source, drain, and gate electrodes was fixed, while zero-derivative boundary conditions were applied at non-contact surfaces. In all simulations, the relative permittivity of the different layers was chosen as $\varepsilon_{r,OSC}$=3.0 in the OSC, $\varepsilon_{r,SAM}$=2.3 in the SAM and $\varepsilon_{r,ox}$=3.9 in the dielectric. The acceptor doping density was set to $N_A=10^{16}$ cm^{-3} in the active region.[37] This value, in comparison to a vanishing doping density, considerably improves the numerical stability of the algorithm. The resulting weakly negatively charged background in the active region was verified not to influence transistor operation, even if the region gets completely depleted of holes.

In equation (1), the initial hole density was set equal to N_A, i.e., $p_0=10^{16}$ cm^{-3} in the whole active region, except for the grid points which represent the source and drain electrodes; there, a constant value according to

$$p_c = N_V \exp\left(-\frac{\Delta_i}{k_B T}\right) \qquad (12)$$

is applied, where N_V is the effective density of states of the valence band (VB) of the OSC and Δ_i is the injection barrier, i.e., the energetic difference between the VB and the Fermi level of the metal contact. According to Scheinert and Paasch,[16] N_V is the monomer density and was set here to a value of 2×10^{21} cm^{-3}. Ohmic contacts are assumed as details regarding the description of the injection process are not within the scope of the present study. This can be guaranteed by setting Δ_i to 0.1 eV, which results in p_c=4.1×10^{19} cm^{-3} at room temperature. In fact, our simulations indicate in accordance to the work of Li et al. [38] that the injection currents become limited only at barriers beyond 0.3-0.4 eV with the consequence that steep potential drops evolve at the contact edges. Assuming an (at least close to) ohmic contact is reasonable, as the experimentally determined injection barrier from Au into P3HT varies between 0.1 eV (for intentionally oxidized Au) and 0.35 eV (bare Au). [39]

The current densities were computed at the half-points of the preset grid, according to a method developed by Scharfetter and Gummel.[40] Perpendicular to non-contact boundaries of the active region, the current density was set to zero. In the sections 3.1 and 3.2, the constant mobility was μ=4.0×10^{-4} cm^{2}V^{-1}s^{-1}.

In order to incorporate the effect of rechargeable trap states (section 3.3), the continuity equation (1) and the Poisson equation (3) were extended to

$$\frac{\mathrm{d}p}{\mathrm{d}t}+\frac{1}{e}\nabla\cdot\mathbf{j}(p,\mathbf{E})=G(p)-R(p) \qquad (13)$$

and

$$\nabla\cdot\left[\varepsilon_r\nabla\varphi\right]=\frac{e}{\varepsilon_0}\left[N_A-p-\frac{N_{fix}}{e}+T_{occ}(t)\right] \qquad (14)$$

Here, $G(p)$ and $R(p)$ are the local generation and recombination rates of holes and $T_{occ}(t)$ is the corresponding density of occupied traps. Note that $T_{occ}(t)$ has the same sign as N_A in the Poisson

equation, which expresses that electron acceptor traps above the VB-edge are modeled (corresponding to hole donor traps). They are neutral if empty (occupied by a hole) and negative if occupied by an electron (in that case, a hole was released to the VB). Only thermal generation of carriers is considered. The generation and recombination rates are modeled according to[41]

$$G(p) = c_t \exp(-\frac{\Delta E}{k_B t})[N_V - p][N_t - T_{occ}]$$
$$R(p) = c_t p T_{occ} \quad (15)$$

Here, c_t is a transition rate between the VB and the trap level, ΔE is the corresponding energy difference and N_t denotes the density of traps at this energy level. The transition rate c_t is the product of the capture cross section σ_c and the thermal velocity v_{th} of the holes and was set to c_t=10^{-12} cm^3s^{-1}.[16,42] The time evolution of the trap occupation was then modeled via

$$\frac{dT_{occ}}{dt} = G - R \quad (16)$$

Besides, in section 3.3, a carrier density-dependent mobility according to a model by Pasveer et al. was implemented:[36]

$$\mu(p) = \mu_0 \exp\left[\frac{1}{2}\left(\sigma^2 - \sigma\right)\left(\frac{2p}{N_V}\right)^{\delta}\right]$$
$$\delta = 2\frac{\ln\left(\sigma^2 - \sigma\right) - \ln(\ln(4))}{\sigma^2} \quad (17)$$

Here, μ_0 is a minimum mobility and σ is the width of the Gaussian density of states associated with the VB in units of k_BT. Both quantities were viewed as fit-parameters.

6. Acknowledgement

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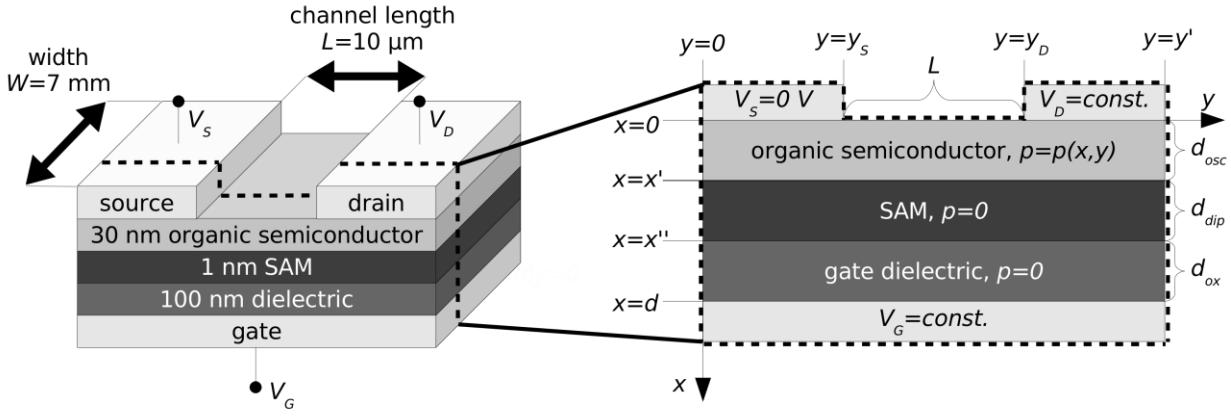

Figure 1. Schematic view of the investigated top-contact transistor structure along with the cross section for which the two-dimensional simulations of the hole transport are performed. *L* is the channel length and *d* is the thickness of the device. A dipolar SAM is modeled by two surface charge densities of opposite signs at *x'* and *x''*, respectively. The density *p(x,y)* of mobile carriers is considered non-zero in the organic semiconductor only.

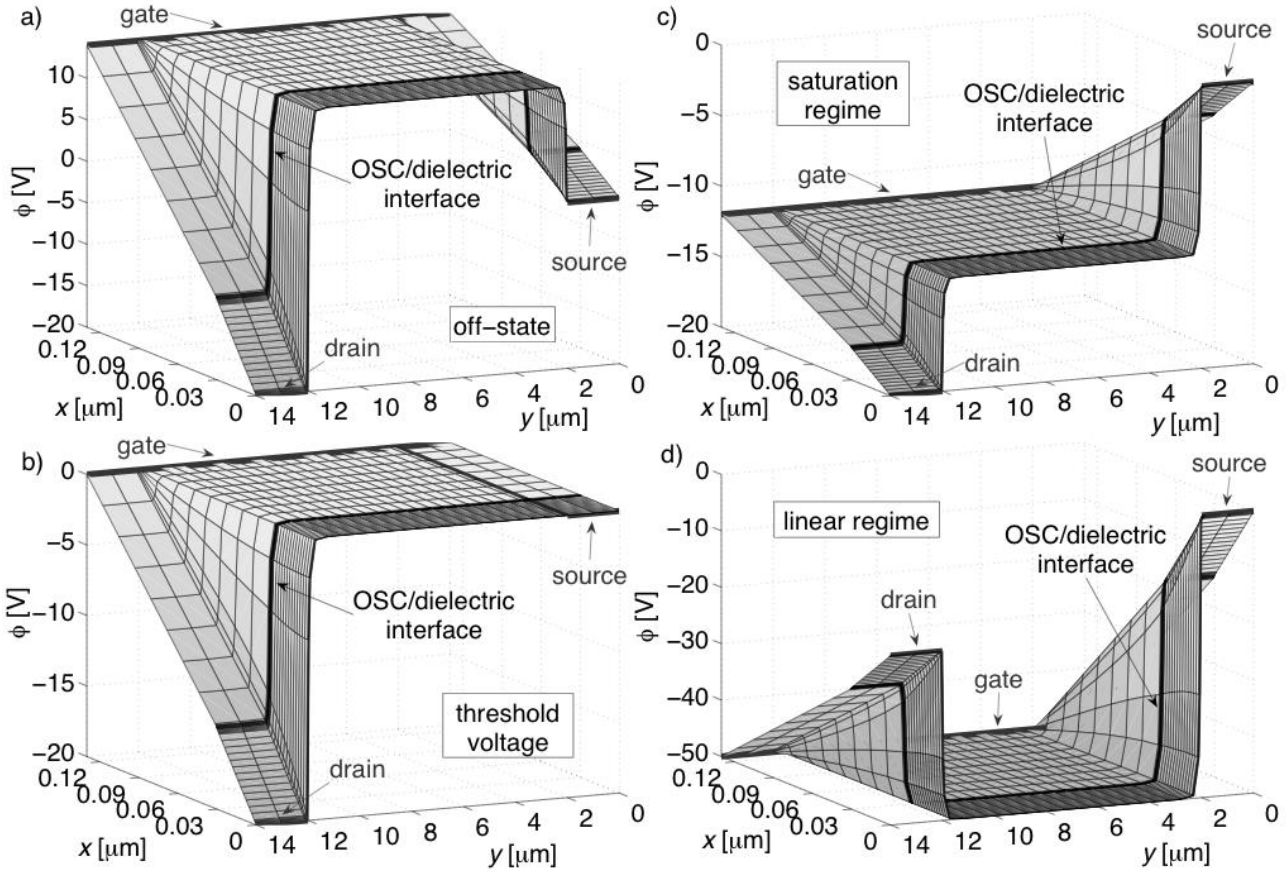

Figure 2. Simulated electric potential profiles of the pristine OTFT with L=10 μm, d_{osc}=30 nm and d_{ox}=100 nm before charge carriers (holes) enter the device (charge-neutrality). The source potential is set to 0 V and the drain potential to -20 V. The gate potential is chosen to represent a) the off-state (+14 V), b) the on/off threshold (0 V), c) the saturation regime (-12 V) and d) the linear regime (-50 V). Geometry setup: gate electrode at x=0.13 μm and 0<y<14 μm; dielectric at 0.03 μm<x<0.13 μm and 0<y<14 μm; OSC/dielectric interface at x=0.03 μm and 0<y<14; OSC at 0<x<0.03 μm and 0<y<14 μm; source electrode at x=0 and 0<y<2 μm; drain electrode at x=0 and 12<y<14 μm

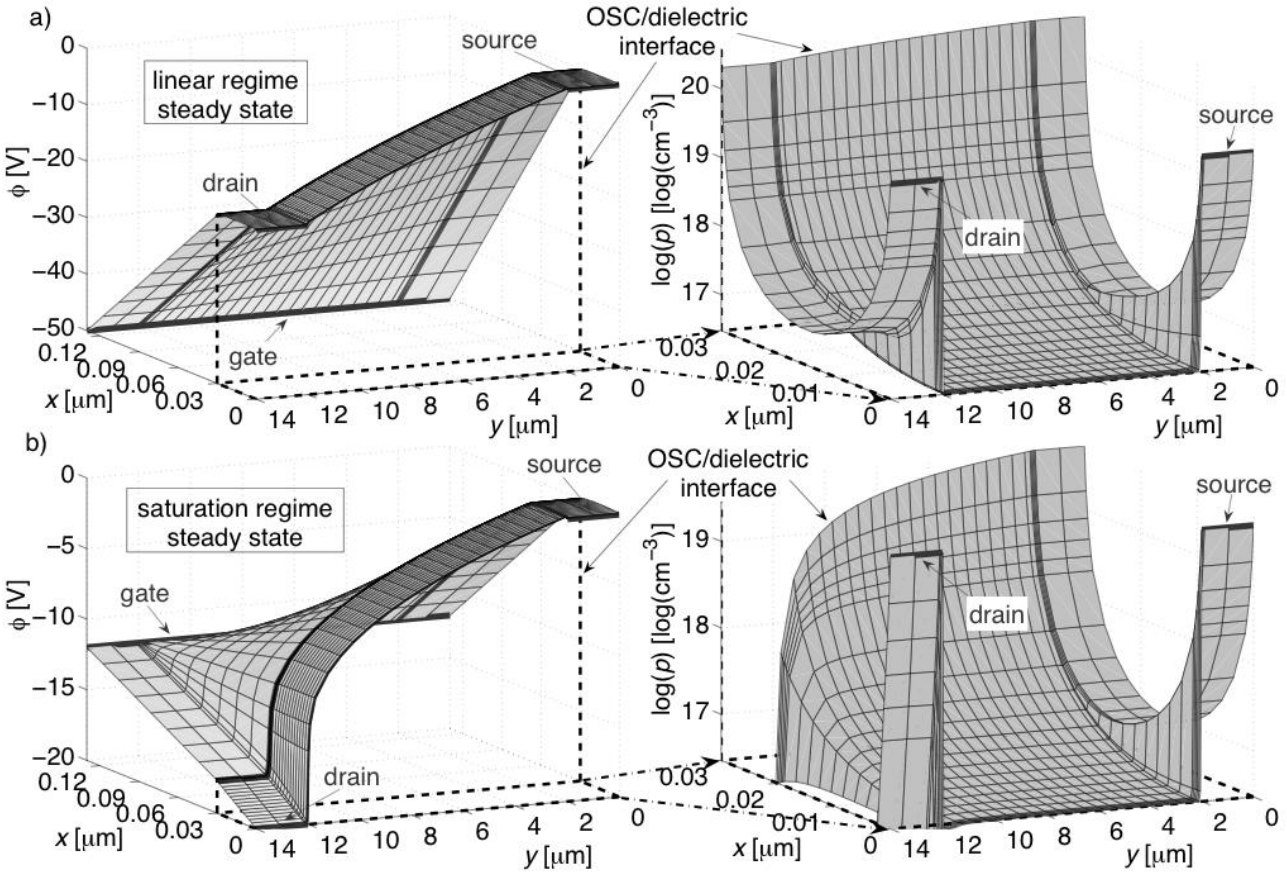

Figure 3. Simulated steady state of the electric potential and the hole density of the pristine OTFT in the linear regime (V_G=-50 V), shown in a), and in the saturation regime (V_G=-12 V), shown in b). The hole density is depicted for the active region only.

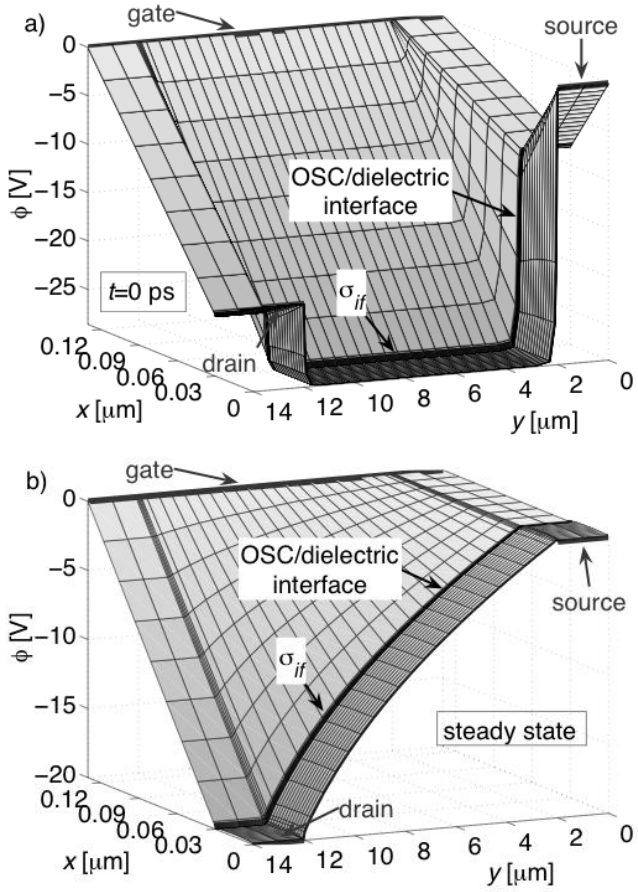

Figure 4. Simulated electric potential of an OTFT in the geometry of Figure 3 with a fixed surface charge of σ_{if}=-6×10^{12} ecm^{-2} at the OSC/dielectric interface at zero gate voltage a) in absence of mobile charges and b) in steady state. The source potential is set to 0 V and the drain potential is -20 V.

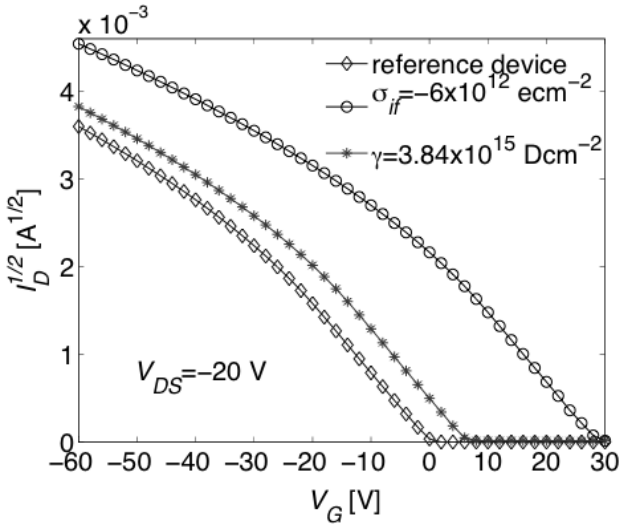

Figure 5. Simulated square root of the drain current vs. the gate voltage of an OTFT with different interface properties, namely a 'clean' interface (pristine reference device), a space charge layer σ_{if} and a dipole density γ.

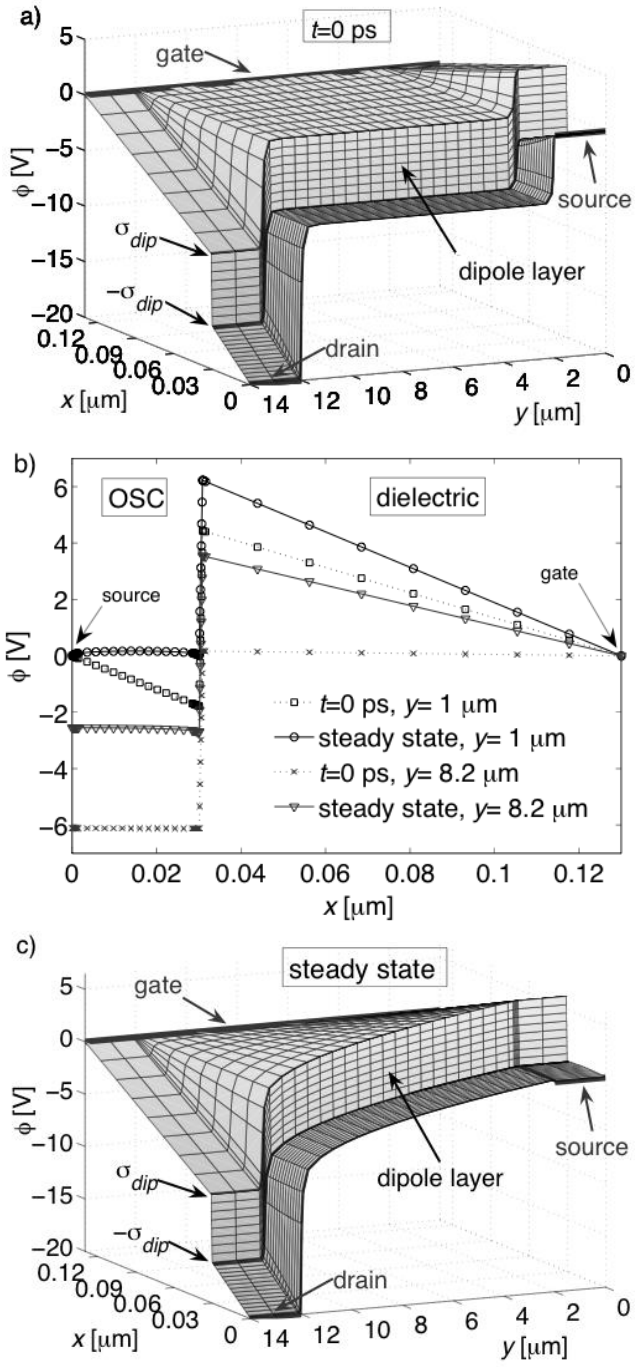

Figure 6. Simulated electric potential a) in the absence of mobile charges and c) in steady state of an OTFT in the geometry of Figure 3 with a polarized layer of γ=3.84×10^{15} Dcm^{-2} at the OSC/dielectric interface. The layer was realized by two surface charge densities σ_{dip}=±1.0×10^{14} ecm^{-2} of opposite sign at a distance d_{dip}=0.8 nm at x=0.03 μm. Source and gate potentials are set to 0 V and the drain potential is -20 V. In b), cross sections of the potentials from a) and c) perpendicular to the transistor surface (i) under the source contact (y=1 μm) and (ii) in the channel (y=8.2 μm) are depicted.

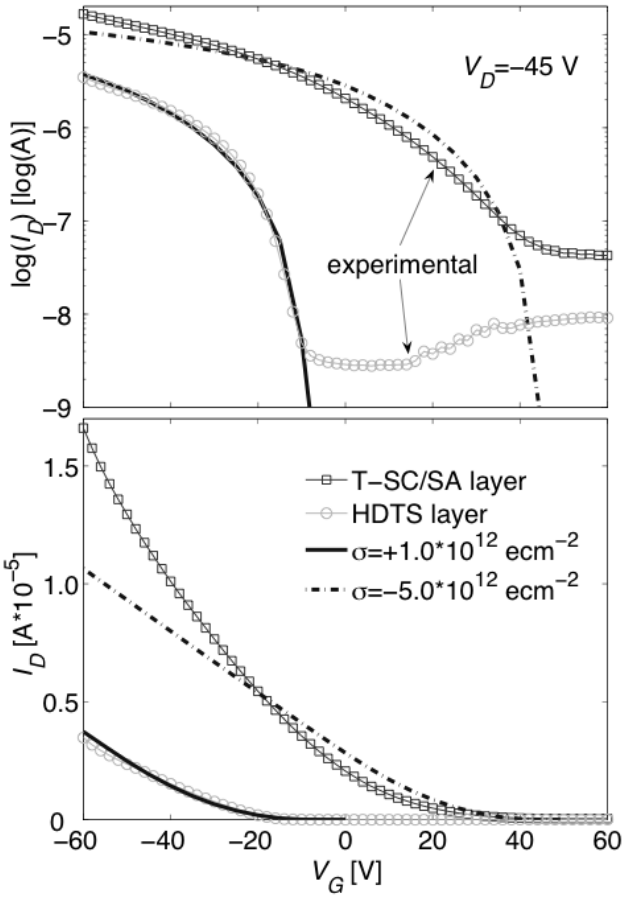

Figure 7. Logarithmic and linear plot of transfer characteristics of OTFTs with different SAMs at the dielectric surface, measured by Pacher et al.[8] The lines without markers are simulation results obtained with a constant mobility and a permanent interface charge density σ_{if}.

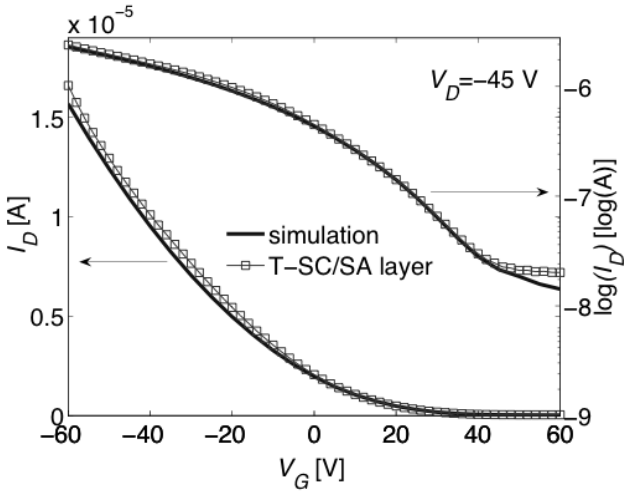

Figure 8. Comparison between the measured and the simulated transfer characteristic of an OTFT with a T-SC/SA layer at the dielectric surface. Rechargeable interface traps and a carrier density-dependent mobility are taken into account in the simulation.

Table 1. Comparison of the threshold voltage shifts ΔV_{th_sim} obtained from simulated transfer characteristics with the effective gate voltage V_{eff} at V_G=0 V calculated from Equation (8) for an OTFT with d_{ox}=100 nm and $\varepsilon_{r,ox}$=3.9 and for different fixed surface charge densities σ_{if} at the OSC/dielectric interface.

σ [10^{12} ecm^{-2}]	ΔV_{th_sim} [V]	V_{eff} [V]
+6.0	-28.6	-28.3
+4.0	-19.0	-18.9
+2.0	-9.3	-9.4
0.0	0.1	0.0
-2.0	9.5	9.4
-4.0	19.1	18.9
-6.0	28.7	28.3

Table 2. Comparison of the threshold voltage shifts ΔV_{th_sim} obtained from simulated transfer characteristics of the regarded SAM-modulated OTFT with the potential drop $\Delta\varphi_{dip}$ over a dipole density γ calculated from equation (11). The absolute value of the corresponding dipole moment M_{dip} of a single molecule of the layer is obtained from equation (6) assuming a molecular 'footprint' A=25 Å^2.

γ [10^{15} Dcm^{-2}]	$\lvert M_{dip}\rvert$ [D]	$\Delta\varphi_{dip}$ [V]	ΔV_{th_sim} [V]
19.19	47.97	-31.4	-31.1
3.84	9.59	-6.3	-6.2
1.92	4.80	-3.1	-3.0
-1.92	4.80	3.1	3.2
-3.84	9.59	6.3	6.3
-19.19	47.97	31.4	31.6

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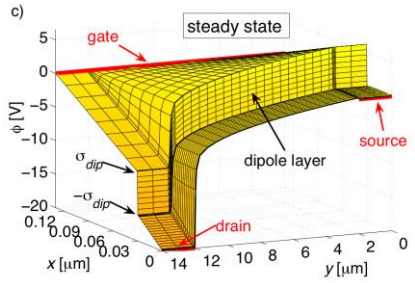
The impact of self-assembled monolayers (SAMs) at the organic semiconductor-dielectric interface in organic thin-film transistors is quantitatively described by means of two-dimensional simulations. It is shown that realistically chosen molecular dipole densities at the interface lead to threshold voltage shifts not exceeding 2 Volts, while a partial ionization of the SAM can give rise to shifts of several tens of Volts.

Keyword (see list)

S. K. Possanner, K. Zojer,* P. Pacher, E. Zojer, F, Schürrer*■<B>…<B>■

Threshold Voltage Shifts in Organic Thin-Film Transistors due to Self-Assembled Monolayers at the Dielectric Surface



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